An Improved Four TFT Circuit for Active-Matrix Organic Light Emitting Diode (AM-OLED) Display

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CERTIFICATE

This is to certify that the work presented in the thesis titled "**An Improved Four TFT Circuit for Active-Matrix Organic Light Emitting Diode (AM-OLED) Display**", by S.K. Bhowmick (Roll No. Y010437) has been carried out under my supervision and that this work has not been submitted elsewhere for a degree.

2nd January 2002

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Finally I wish to convey my gratitude to my parents and my family for being the continuous source of support and inspiration to me.

Soumitra K. Bhowmick

ABSTRACT

Active Matrix OLED (AM-OLED) displays are being actively developed as the flat panel display technology of the future due to their several advantages including wide viewing angle, fast response time, thin size and low cost. For the success of AM-OLED display, it is important that the pixel characteristics be independent of variations in OLED and TFT characteristics. The pixel circuits proposed so far achieve this requirement but suffer from low output current range. In this work, we show that the output current range can be enhanced threefold by minimizing clock feedthrough effects through proper transistor sizing. We also propose a new pixel circuit with high output current range and less number of control signals using four polysilicon TFTs. Good performance was obtained for output currents as high as 25μA thereby making the pixel circuit suitable for high-resolution OLED displays.

Dedicated to

Manju and Shibendu

for being so patient and lovingly

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Chapter - 1

INTRODUCTION

Organic Light Emitting Diode (OLED) displays are being actively developed as the Flat Panel Display (FPD) technology of the future since the first report of efficient light emission from organic small molecule by **[1]** Tang et. al. OLED displays possess all the features necessary to be the dominant FPD technology: low cost, low power consumption, high brightness, full color, wide viewing angle and the ability to be made on flexible substrates. In future OLED displays are likely to replace Liquid Crystal Displays (LCDs) in applications ranging from cellular phone displays to high information content Laptop Computers due to it's superiority over LCD displays. Recently, Sony has developed a 13-inch active matrix OLED display using its novel TAC (TAC: Top emission Adaptive Current drive) technology. That display is a little thicker than a credit card and has the potential to replace the bulky TV tube **[2]**.

In general, OLEDs are organized in a matrix structure of Rows and Columns. Each pixel is electrically connected between one Row lead and one Column lead as shown in **Figure 1.1**. The addressing of large number of pixels in matrix-addressed displays is an important issue in display technology **[4]**. For applications that require low information content display the relatively simpler Passive Matrix (PM) addressing scheme can be used. They are generally referred as PM-OLED displays **[3]**. However, for the high information content, high-resolution display applications, it becomes necessary to use Active Matrix (AM) addressing scheme. In AM addressing scheme, OLEDs are integrated with active electronic components like Metal-Oxide-Semiconductor Field Effect Transistor (MOSFET) or Thin Film Transistor (TFT) in a suitable manner. In PM addressing no such active components are used and hence the name 'passive' used here.

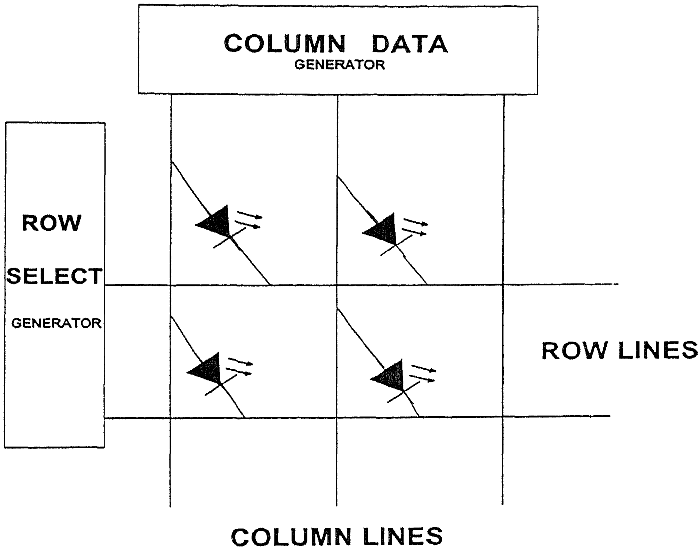


Figure 1.1: Matrix Structure of OLED display

The circuit design issues for AM-OLED displays are challenging in the sense that various device non-idealities and mismatches are to be taken care of through the design techniques. For large FPDs thin film transistors are likely to be used rather than MOSFETs. The TFT non-idealities include spatial threshold voltage variation (ΔV_{th}) of the order of millivolts, mobility variation and subthreshold swing. Of all these, the threshold voltage variation is most critical. Basically OLEDs are current driven devices. In AM-OLED display, the threshold voltage variation causes non-uniformity in the output current of the TFTs, which in turn causes, non-uniformity in the image being displayed. The increase in OLED's turn-on voltage due to aging also contributes to image non-uniformity. The important issue in pixel circuit design therefore involves minimization of the non-uniformities in the image being displayed by adjustment for the above mentioned variations.

1.2. Literature Review

The simplest two TFT based AM-OLED pixel suffers from the problem of image non-uniformity [5] due to spatial threshold voltage variation (ΔV_{th}) of the driving TFTs

across the display panel. Till today various schemes (using more than two TFTs) have been proposed to tackle this problem **[6-10]**. For the case, where the pixels are driven by current source **[6-8,10]**, all the solutions are based on analog switched-current memory cells **[11]**. While in **[10]** P-type Polysilicon (p-Si) TFTs were used, in **[6-8]**, N-type hydrogenated amorphous silicon (a-Si:H) TFTs were used. The image non-uniformity due to the threshold voltage variation is practically eliminated in these circuits but they have limited output current range over which the output current matches well with the input (data) current. The circuits proposed in **[5]** are large hardware oriented and will limit the pixel fill-factor.

For the circuit where OLED is driven by voltage source, the complexity in the driving waveforms is quite high. In the schemes proposed **[9,18]** the driving TFT's threshold voltage along with OLED voltage is measured and stored in a capacitor using an autozero cycle first. The data voltage is then applied to the gate of the driving TFT. Since the gate-to-source voltage of the driving TFT develops over the already stored voltage due to threshold voltage, the output current becomes independent of the threshold voltage variation of the driving TFT.

Another solution proposed **[12]** by Hack et. al. suggested the use of digital processing along with much simpler two TFT pixel to eliminate the image non-uniformity. In this approach, each pixel is calibrated by measuring the OLED current as a function of data voltage and then storing the current-voltage (I-V) characteristics in a Look-up table. When a specific pixel is to be addressed the driving electronics determine the required OLED current from the brightness of the visual image and the look-up table is accessed to determine the necessary data voltage. This ensures that the OLED current is not dependent on the uniformity of either the TFT or the OLED characteristics.

1.3. Scope of the Thesis

The AMOLED displays require pixel circuit, which while using minimum number of transistors (minimum area) should also compensate for the variations in OLED and TFT characteristics. The other important aspect is to have a large output current range so as to achieve large number of gray levels for high-resolution displays without the expense of larger area of the pixel circuit.

The pixel circuits proposed so far achieve this requirement but suffer from less output current range. . In this work, we show that the output current range can be enhanced threefold by minimizing clock feedthrough effects through proper transistor sizing. We also propose a new pixel circuit with high output current range and less number of control signals using four polysilicon TFTs. Good performance was obtained for output currents as high as 25μA thereby making the pixel circuit suitable for high-resolution OLED displays.

1.4. Organization of the Thesis

The thesis is organized in four chapters. In **Chapter 2**, the brief overview of OLED display is presented. This chapter deals with the display element, display addressing and driving devices for high-resolution OLED displays. The core of the thesis lies in the **Chapter 3**, where the actual designs of the pixel circuits are unfolded. Various improvement factors are also brought out there. The results are presented and analyses of the results are done to have better understanding of the pixel circuits. Finally, **Chapter 4** concludes the details of the study and emphasizes the scopes for future extension of the research.

Chapter - 2

OLED DISPLAY : A BRIEF OVERVIEW

2.1. Introduction

The major motivation to replace LCDs with OLEDs in future stems from various advantages that they provide like light-weight, low-power, high resolution, emissivity etc., to name a few. OLEDs produce light based on the current applied to its terminal, whose brightness is function of the applied current density. Recent progress [4] in the OLED research significantly improved the OLED efficiency, which makes it possible to achieve high brightness with much smaller current (~few μA). It is also possible to design full-color display using three basic color OLEDs in a suitable manner. Thus, with the availability of OLEDs with high brightness, useful color combination and long lifetime, it is possible to construct FPDs with arrays of OLEDs. Although low-resolution displays are useful, the possibility of constructing high-resolution displays is of great interest to industry and academia. Such displays would be an attractive alternative to Active Matrix LCDs (AMLCDs) especially because they would greatly eliminate the viewing angle problems and would reduce the cost factor and system size by eliminating the display backlight.

For achieving high resolution, large area FPDs using OLEDs, it is important to understand all the important elements of the display. The present chapter describes in brief the OLED, transistor and driving scheme used in these displays

2.2. OLED and PLED as display element

The OLEDs are basically diodes, which emit light proportional to the drive currents. The structure of a conventional OLED [4] is shown in **Figure 2.1**. The electrons and holes are correspondingly injected from the cathode and anode and migrate through the electron and hole transport layers. Organic EL is obtained simply by placing a charge-

transporting and light-emitting organic material between two electrodes (one of which is transparent) and applying a suitable bias. The organic material may be either a polymer, deposited by various solution processing techniques, or low molecular weight molecules (commonly called "small molecules"), deposited by evaporation in vacuum. Total device thickness (excluding the substrate) is less than 1 micron. When biased, charge is injected into the highest occupied molecular orbital (HOMO) at the anode (positive), and the lowest unoccupied molecular orbital (LUMO) at the cathode (negative), and these injected charges (referred to as "holes" and "electrons," respectively) migrate in the applied field until two charges of opposite polarity encounter each other, at which point they annihilate and produce a radiative state.

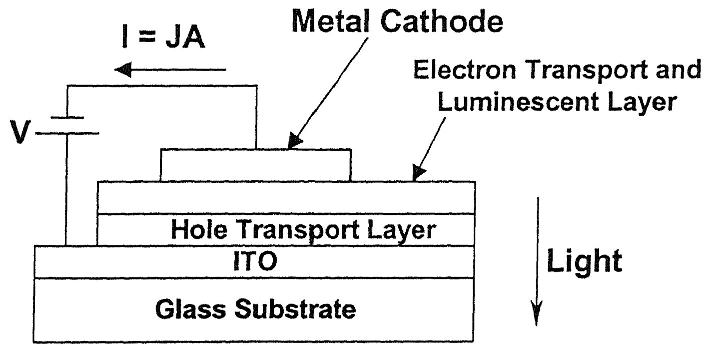


Figure 2.1: OLED/PLED Structure

C.W. Tang and S. VanSlyke [1] at Kodak [3] introduced the double layer concept in 1987, which worked for a moderately low bias voltage with attractive efficiency, and encouraging lifetimes. Their devices were made by subliming molecules of a triarylamine as hole transporter, followed by aluminato-tris-8-hydroxyquinolate (Alq3) for electron injection and emission, and a magnesium-silver alloy cathode. In 1990 J. Burroughes, et al.[17], reported a similar device made with a polymeric medium: poly(phenylene vinylene) (PPV). It consists of a thin layer of undoped conjugated polymer sandwiched between two electrodes on top of a glass substrate. In double layer polymer LED(PLED) the electron transport layer used is CN-PPV whereas hole transport layer used is MEH-PPV.

2.3. OLED Display Matrix Addressing Schemes

OLED display is essentially an array of independently controllable pixels, the number of which depends on its dimension and resolution required by a particular application. Very large pixel counts are encountered in high information content displays. For example, an NTSC standard TV screen requires 1.5 $X10^5$ pixels. The addressing of large number of pixels in an array is an important issue in display design. In a matrix addressed display, operation of each row is sequentially **[Figure 1.1]** activated, where the pixels in the selected row are activated using the corresponding column lines.

2.3.1. Passive Matrix OLED Display

A passive matrix OLED (PM-OLED) array consists of two sets of electrically isolated leads (Rows and Columns) arranged in orthogonal with an OLED at each intersection as shown in **Figure 2.2**. An electronic switch is employed to address each of the rows. To achieve gray-levels, the column drivers must be current sources of varying strengths.

In passive matrix addressing, unintentional direct coupling occurs when pixels in different rows are simultaneously addressed. To prevent this the array must be addressed pixel-at-a-time or row-at-a-time. The row-at-a-time is generally chosen to maximize the pixel duty factor. The pixel duty factor is defined as the percent of the total time each pixel is driven into the ON State by the column signal. If there are 'M' rows in the display then 1/M is the pixel duty factor for row-scanned array.

Also a large number of pixels are unintentionally reverse biased when a pixel is addressed. To prevent this, the addressed pixels must be driven with a pulsed current source to avoid the catastrophic and irreversible breakdown or shortening caused by long time reverse bias on the non-selected pixels. Since the pulsed operation for short duration has to produce an average display brightness or luminescence, the number of rows in a passively addressed display is limited.

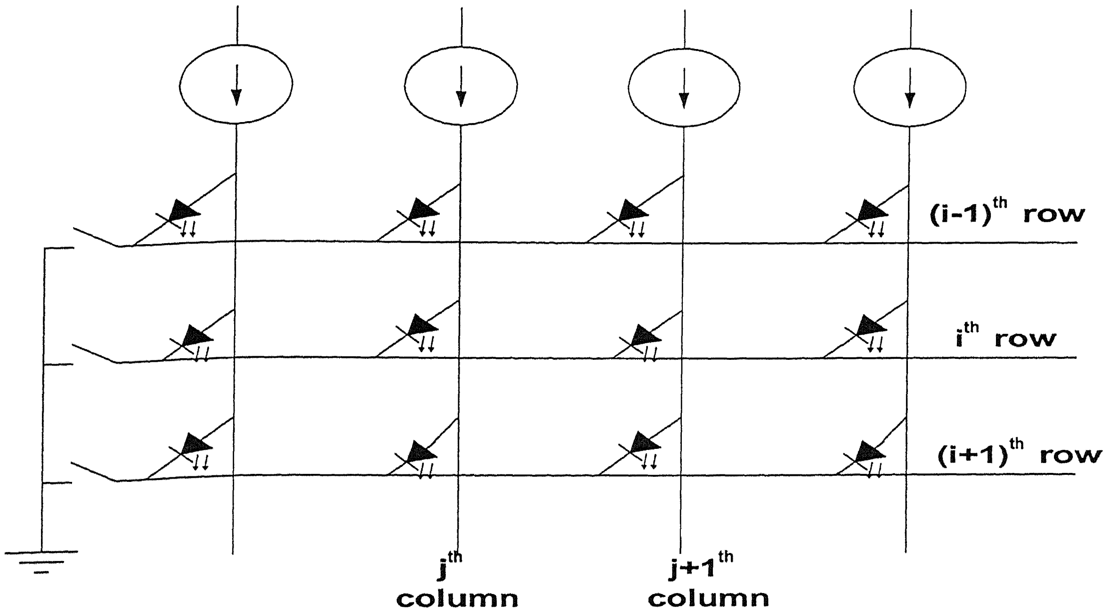


Figure 2.2: Passive Matrix OLED addressing

Thus, we see that the PM-OLED arrays have the merits of being simple and easy to fabricate but plagued by limitations of the display size due to the following factors :

- The high instantaneous pixel luminescence required to achieve a given average display brightness due to the very low pixel duty factor, limiting the number of rows to below 1000 [4].
- The leakage current through the non-selected pixels limits the display size and
- The voltage drop across the column and row lines, limits the display dimension to below 40cm in width and height or (17 inch in diagonal)

Due to all these limitations, Active Matrix addressing is necessary for high information content, large area FPDs.

2.3.2. Active Matrix OLED Display

In the Active Matrix OLED (AM-OLED) display active matrix addressing is used. In this addressing scheme an electronic switch (T1) is placed at each pixel providing the means to retain the video information on a storage capacitor (C_S) during the complete frame time. An additional active component (T2), known as drive transistor is needed to provide the OLED with drive current at each pixel. These active components are Field Effect Transistors such as MOSFETs or Thin Film Transistors (TFTs) depending on the application. The channel material of the TFTs can be Polysilicon or amorphous silicon or even organic small molecules.

The simplest AMOLED pixel circuit is shown in **Figure 2.3**. The circuit works as

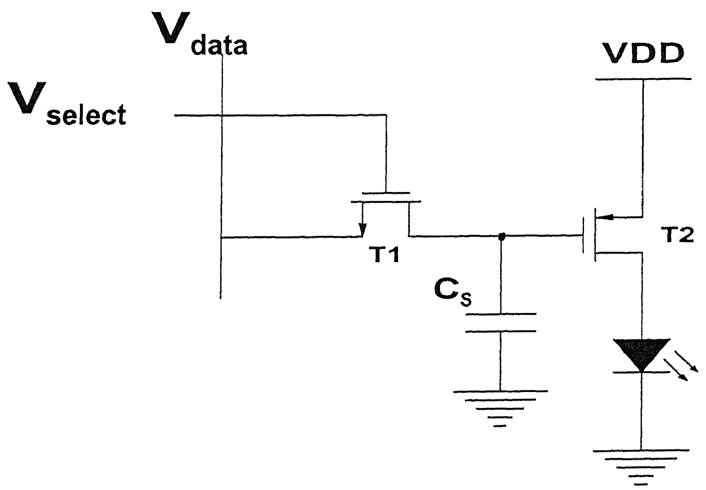


Figure 2.3: Simple AMOLED Pixel Circuit

follows: When the select line V_{select} (row) is made high ('1') the data voltage from column signal (V_{data}) is written via the access transistor T1 to the gate of driver transistor T2. The written voltage V_{G2} is thereby retained for a complete frame time (T_f). T2 is made to operate in saturation regime, where the OLED drive current is controlled by the gate-to-source voltage V_{GS2} and has little dependence on source-to-drain voltage V_{DS2}.

The AM addressing scheme actually eliminates all the drawbacks of passive matrix addressing and opens up the potential to build large area, high information content OLED displays.

2.4. Active Matrix Driving Mechanisms

There are two broad types of active matrix addressing mechanisms

- Digital
- Analog

In the Digital driving methods an electronic switch is used with each OLED. There are various gray-scale generation methods like Area ratio gray-scale and Time ratio gray-scale.

In Area ratio gray-scale method, the number of gray-scales is proportional to the total number of sub-pixels of equal size that can be connected to the applied voltage. Transistors are used to select the number of sub-pixels to be lit up at a particular time **[5]**. To reduce the number of signal lines, OLEDs with binary weighted areas are used. This method allows lower operating voltage and gives more accurate gray-scale. But the number of sub-pixels per pixel, for large number of gray-scales becomes very large. This also results in a large increase in the number of signal lines.

In Time ratio gray-scale method, the frame period is divided into a number of sub-frames of binary weighted duration. This can be achieved by processing the data signal at source and deliver it to the OLED at high data rate. However for 8-bit gray-scale, the data rate will be increased by a factor of 256. The power loss at high switching frequency is significant due to the stray capacitance of the common ground plane (cathode).

In the combination of Area with Time ratio method, the number of gray-scales can have significant increment. This seems the most promising digital pixel driving method. The OLED and the sub-pixel driver circuit determine the area of each sub-pixel. The display resolution, the total number of gray-scales and the power consumption requirement determine the optimum number of gray-scales to be generated by area ratio and time ratio method. This in turn fixes the final display panel size.

In the analog methods, each OLED is driven by a controlled current source. The controlled current source can be programmed by using either a current source or a data voltage source and should provide desired current throughout the frame time

corresponding to the gray-level. For this the right driver transistor is to be selected and accompanying circuit is to be configured to provide constant current to the OLED. The spatial threshold voltage variation in the driver transistor may cause non-uniformity in the image due to the output current error in the pixel circuit. This issue is discussed in detail in chapter 3.

2.5. Active Matrix Driving Devices

In principle, any FET like MOSFET or TFT can drive the active matrix OLED display. However, the MOSFETs can be used only for very small character type display. For large area displays, TFTs fabricated on the display panel itself is the only alternative.

TFTs which use Polysilicon as the active channel material, are known as Polysilicon (P-Si) TFT, whereas TFTs, which use amorphous silicon as the active channel material, are known as Amorphous-Silicon (a-Si) TFT. The electrical characteristics of these two types of TFTs differ from each other, which is to be taken care of during circuit design. Also Organic TFT (OTFT) is being actively developed and has shown reasonable performance to be feasible as active element in AM-OLEDs.

2.5.1. Amorphous Silicon TFT

Hydrogenated amorphous silicon TFT (a-Si:H) is largely used in Active Matrix Liquid Crystal Displays (AMLCDs). It is a very low cost and mature technology that can be fabricated over a large area. The structure of a-Si:H TFT is shown in **Figure 2.4.**

The amorphous silicon has large number of localized states distributed throughout the forbidden gap, which makes the operation of this TFT different from the crystalline MOSFET. One of the effects of this disorder is very low field effect mobility of the order of $1 cm^2/V$-sec. From the physics point of view **[13]**, the electron transport in the channel of these devices can be visualized as electrons travelling a short distance while in the conduction band and then being trapped, then re-emitted into the conduction band and so on.

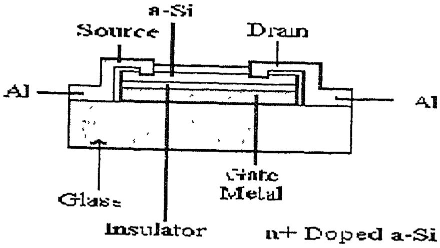


Figure 2.4: Amorphous Silicon TFT Structure

With the advent of high efficiency Electro-phosphorescent OLEDs, a-Si:H TFTs can be used as active elements in AMOLEDs. The disadvantage is that P-channel a-Si:H TFT has got very low mobility and is thus not used. Thus CMOS type circuits are not possible using a-Si: H TFT.

2.5.2. Polysilicon TFT

The P-Si TFTs provide much higher mobility (~100 cm^2/V-sec) than a-Si:H TFTs but also cost a lot. Both P-type and N-type TFTs are available using Polysilicon technology. This provides means to design high performance CMOS circuits. The structure of Polysilicon TFT is shown in **Figure 2.5.**

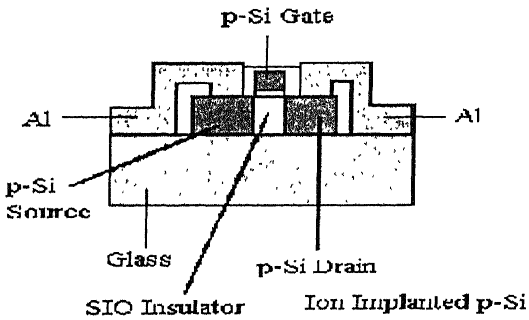


Figure 2.5: Polysilicon TFT structure

The Polysilicon TFTs are fabricated using poly-crystalline silicon films. The operation is very similar to its crystalline counterpart. However gate oxide of Polysilicon is deposited rather than grown. The difference in Polysilicon TFT and crystalline MOSFETs

are related to the presence of grain boundaries in the polysilicon material. They act as barriers to the charge carriers and also contain dangling bonds and other types of traps. The field effect mobility varies between thirty to few hundred cm^2/V-sec.

2.5.3. Organic TFT

Organic TFTs use organic semiconductors as the active layer material. This may offer significant processing advantage in building OLED displays. The performance of OTFTs in terms of higher field effect mobility and lower threshold voltage has improved a lot in recent years **[14]** and has rapidly approached to that of a-Si:H TFTs. While several organic materials for active layers are being extensively investigated, the OTFTs fabricated with small molecule pentacene **[15]** has shown the best performance. The structure of an OTFT, using pentacene as active material is shown in **Figure 2.6.**

Pentacene is a short chain molecule consisting of five linearly fused benzene rings. It is typically used as P-type organic semiconductor. Pentacene based TFTs have been demonstrated **[15]** to with –2 Volts threshold voltage, 0.7 Volts/decade subthreshold slope and ON/OFF current ratio larger than 10^8 making them suitable for all organic display.

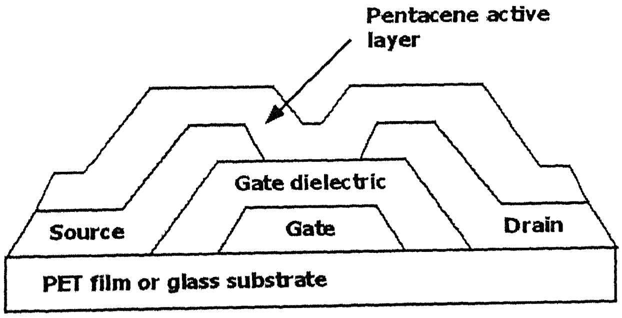


Figure 2.6: Pentacene based OTFT structure

The OTFTs are generally P-type and can be integrated with N-type a-Si:H TFTs to get CMOS circuits **[16]** fabricated on the display panel for driving electronics. The mobility of these devices matches well along with other operation characteristics like supply voltage and threshold voltage.

Chapter - 3

DESIGN AND SIMULATIONS OF THE ACTIVE MATRIX PIXEL CIRCUITS

3.1. Introduction

The active matrix pixel circuits can be classified into two broad categories based on the type of input data. The first one is the Voltage pixel circuit, while the second one is Current pixel circuit. In either case the light output from the OLED is proportional to the current that passes through it. This is schematically shown in **Figure 3.1**. In **Figure 3.1(a)** OLED is driven by a voltage source. A current flows through the OLED on applying a bias voltage at least equal to the turn on voltage of the OLED. The current driven circuit is shown in **Figure 3.1(b)**, where the current first charges up the associated parallel capacitance (C_{OLED}) of the OLED and once the turn on voltage is developed current starts flowing through the OLED. Based on the driving signal the voltage driven circuit is known as Voltage pixel circuit and the Current driven circuit is known as Current pixel circuit.

The simplest pixel circuit is voltage driven and shown in **Figure 2.3**. Since the OLED is a current driven device, two transistors are necessary for accessing and driving purposes. The two-transistor scheme, adapted from the AMLCDs is inferior as far as image uniformity is concerned because the threshold voltage variations in the driving transistor produce high non-linearity in output current.

To avoid this problem, there are techniques for compensating the threshold voltage variations. Various techniques have been proposed based on Voltage and Current pixel circuit topologies **[5-10,18]**. The current pixel circuits use four to six transistors to avoid the problem, while voltage pixel circuits use almost same number of transistors but with more complicated driving signals and more than one storage capacitors.

In this chapter the current pixel circuits will be presented first followed by the voltage pixel circuits.

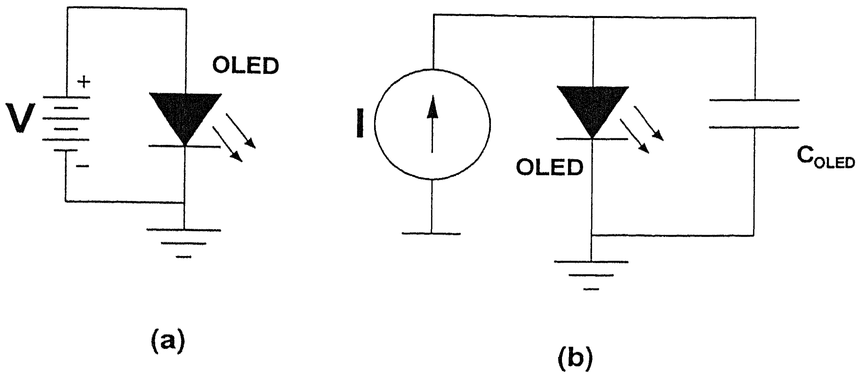


Figure 3.1: OLED driven by voltage (a) and current (b)

3.2. Basic Principle of Operation of Current Pixel Circuit

The basic principle of operation of current pixel circuits [6-8,10] can be traced to the well-known principle of the current copier [11]. The circuit [**Figure 3.2**] of a simple current copier can be used to explain the principle.

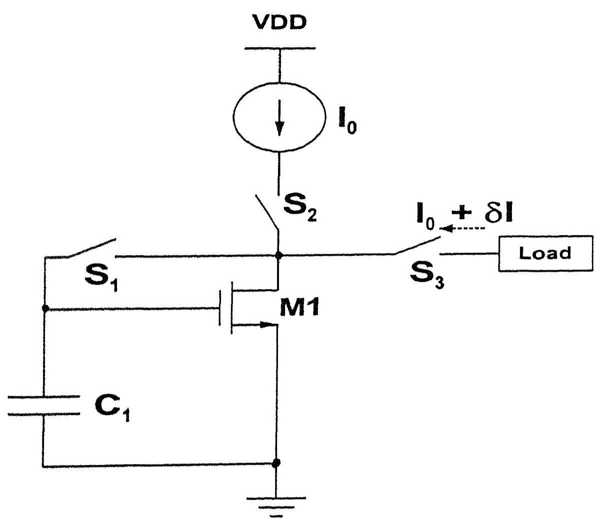


Figure 3.2: A simple current copier

In the programming phase the switches S1 and S2 are closed and gate-to-source voltage of the driving transistor M1 is stored in a storage capacitor (C1). In the reproduction phase, S1 and S2 are opened and switch S3 is closed so that the current to the load is exactly the same as that of the programming current based on the memorized gate-to-source voltage of M1. δI describe the current error due to change in the drain voltage of M1.

This principle can be used to explain the current pixel circuit for AMOLED as proposed in **[6-8,10]**. These circuits use four thin film transistors (TFT1-TFT4). Among them the p-type polysilicon TFT based circuit proposed by Dawson et. al.**[10]** is shown in **Figure 3.3**.

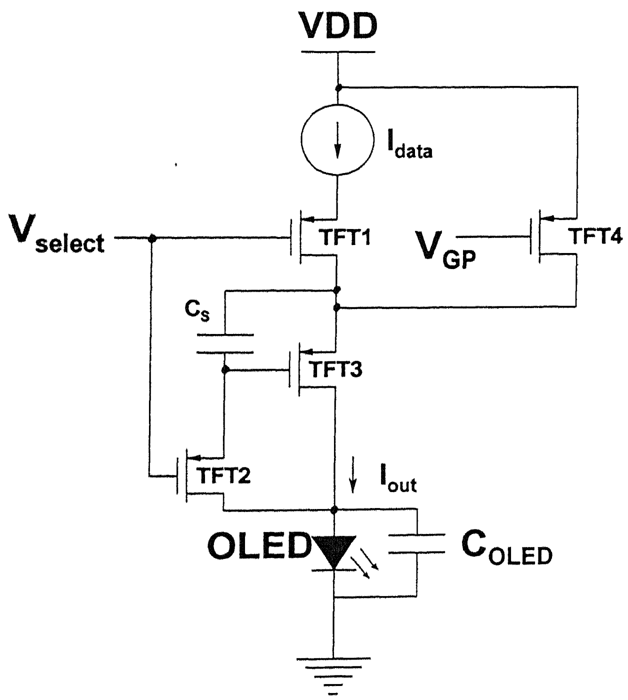


Figure 3.3: P-type TFT based Pixel Circuit

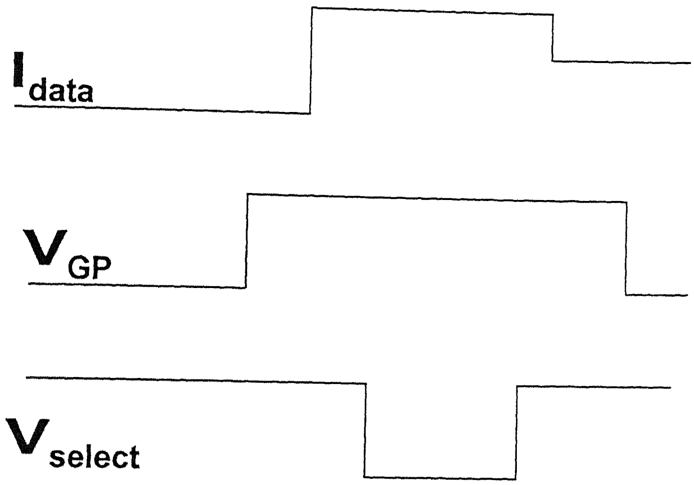


Figure 3.4: Operation waveforms used in the circuit of Fig 3.3

This circuit requires an external source I_{data} for supplying the current data. During the programming stage TFT1 and TFT2 are turned ON, I_{data} passes through the diode connected TFT3 into the OLED. The resulting gate-source voltage of TFT3 is kept by the storage capacitor C_S. During the reproduction stage TFT1 and TFT2 are turned OFF and TFT4 is turned ON. Now TFT4 is connected to VDD and functions as a current source governed by the stored voltage across C_S. Since same transistor (TFT3) is used in both side of a current mirror type configuration, the circuit should be insensitive to the value of threshold voltage variations of the transistor.

There is one more variant of the same type of current pixel circuit using N-type amorphous Silicon TFT, proposed by Hattori et. al [7-8] and shown in **Figure 3.5**. The circuit has five external terminals (VDD, ground, V_{ctl}, I_{data}, V_{select}) of which VDD and ground are common to all the pixels. V_{select} and V_{ctl} are the two control signals, while I_{data} is the input data current pulse. The number of control signals can be reduced to four by using two additional TFTs connected as an inverter to generate V_{ctl} with V_{select} as the input. The circuit has two phases of operation. In the first phase programming is done.

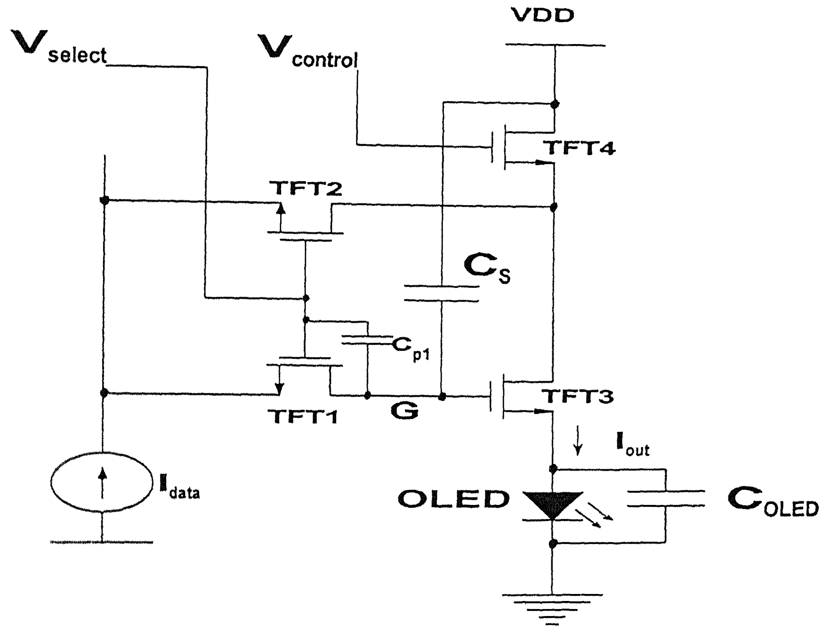


Figure 3.5: Amorphous Silicon TFT based Pixel Circuit

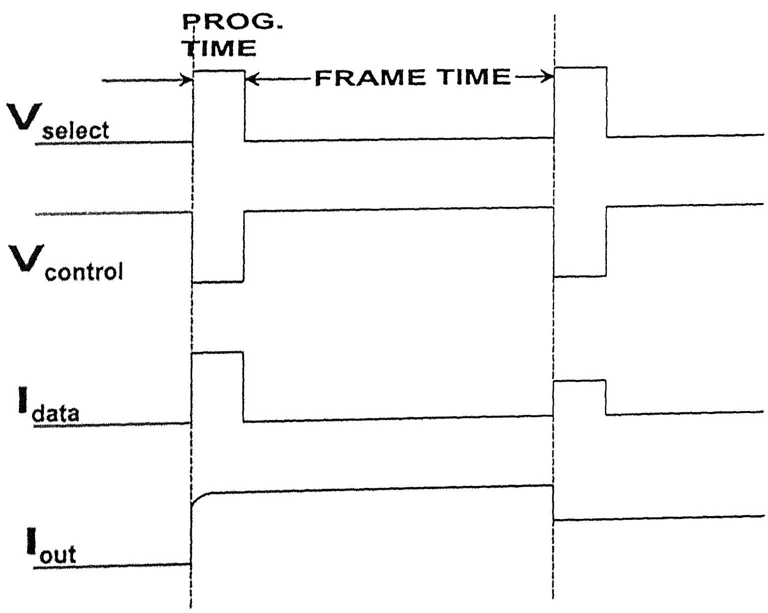


Figure 3.6: Operation Waveform for Pixel Circuit of Fig. 3.5

Programming of I_{data}:

When the select line (V_{select}) is high both TFT1 and TFT2 are turned ON. $V_{control}$ is kept low during this time so that TFT4 is OFF. The data current pulse then passes through TFT1 and TFT2 and sets both the drain and gate voltages of TFT3. The potential at the drain and gate of the transistor TFT3 will allow the data current to flow through TFT3 [**Figure 3.5**]. TFT3 works in saturation regime. Thus the current flowing through TFT3 is equal to I_{data}. The current applied to OLED anode will turn on the OLED and reach the ground.

Reproduction of I_{data}:

When the program current pulse is removed, that is the pixel is deselected, V_{select} lies low and TFT1 and TFT2 turn OFF. The gate voltage of the driving transistor (TFT3) is stored in a storage capacitor (C_S). Now the $V_{control}$ signal is made high to turn ON TFT4 whose drain is connected to VDD. This time the current will flow from VDD to TFT3 via TFT4. If TFT3 gate voltage is maintained and TFT3 is operated in saturation regime, the output current level would be equal to I_{data}. **Figure 3.6** shows the timing waveforms used in the circuit.

In the circuit shown in Figure 3.5, if the threshold voltage of the drive TFT3 changes, it's gate voltage changes accordingly to ensure the same output current level. The threshold voltage variation of other TFTs do not have any major impact on the output current since they are not involved in controlling the current output. The circuit can adjust not only the threshold voltage variations of the driver transistor (TFT3) but also compensate for variations in OLED turn-on voltage **[6]**.

3.3. Simulation results of current pixel circuit

The current pixel circuit **[Figure 3.5]** was simulated using AIM-SPICE circuit simulator using amorphous silicon TFT model (Level 15 ASIA 2 **[11]**). The description and values of the model parameters are given in Table –A1 in **Appendix-A**. The TFT sizes **[8]** are shown in **Table 3.1** along with the capacitor values used for the circuit simulation.

TABLE 3.1: Design Parameters for Amorphous Silicon TFT circuit

VDD = 25 Volts; V_{select} = 0 – 25V ; V_{ctl} = 0-25V; I_{data}= 0-20 μA

TFT1 (W/L)	TFT2 (W/L)	TFT3 (W/L)	TFT4 (W/L)	C_{OLED}	C_S
50μm/6μm	100μm/6μm	250μm/6μm	250μm/6μm	6 pF	6 pF

The OLED was modeled as a gate-drain connected TFT in combination with a capacitance C_{OLED} in parallel as shown in **Figure 3.7** The I-V characteristic of this TFT (W/L=200μm/6μm) emulating OLED is shown in **Figure 3.8.**

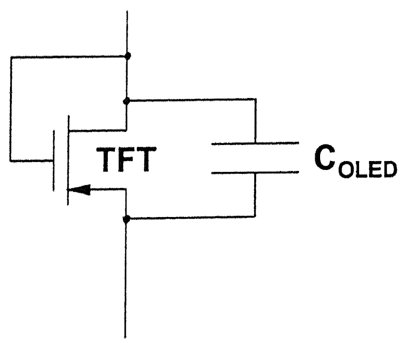
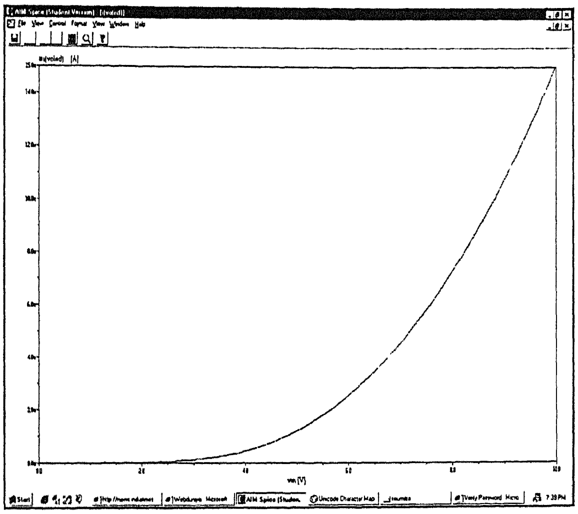


Figure 3.7: TFT emulating OLED

I (μA)



Bias(V)

Figure 3.8. I-V Characteristics of the TFT emulating OLED

Circuit simulations were used to evaluate the circuit performance with respect to two performance parameters : Immunity to threshold voltage variations and output current non-linearity. Simulations were carried out to study first the circuit as reported in **[4-6]** to understand its operation and limitations.

1) Threshold voltage variation of the drive TFT: The threshold voltage of the drive TFT was varied from 1.5 volt to 3.5 volts in steps of 0.1 volt, keeping the threshold voltages of other TFT constant at 2.5 volts. The immunity of the circuit to threshold voltage variation was checked for input data (I_{data}) current of 5μA and is shown in **Figure 3.9** where the percent change in output current is plotted against the percent change in threshold voltage. The data current was pulsed with an ON time of 30μs and OFF time of 300μs corresponding to a display of VGA resolution.

2) Output current non-linearity: The mismatch between data current and output current was studied using the current non-linearity parameter defined below

$$\text{non-linearity} = [(I_{data} - I_{out})/ I_{data}]\ \%$$

where I_{data} and I_{out} are the input data current and output current respectively.

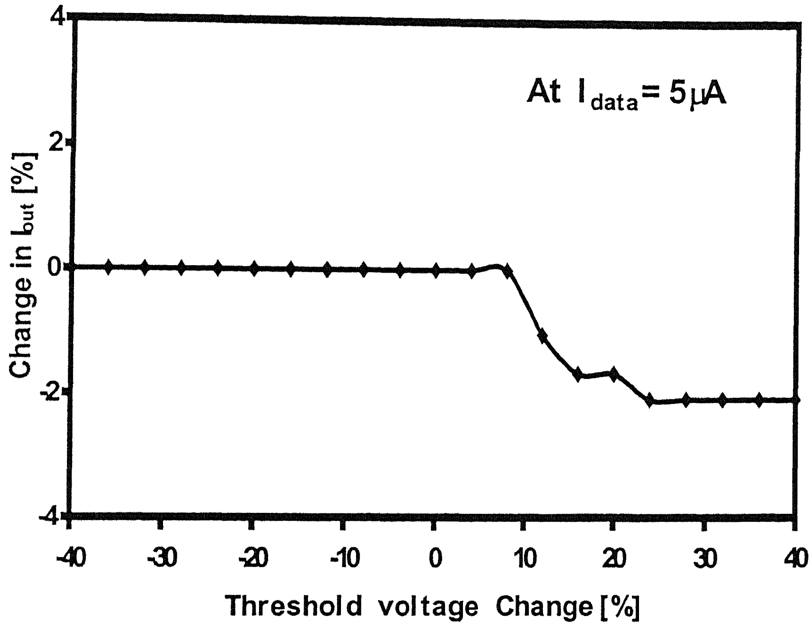


Figure 3.9: Threshold voltage change vs. Change in I_{out}

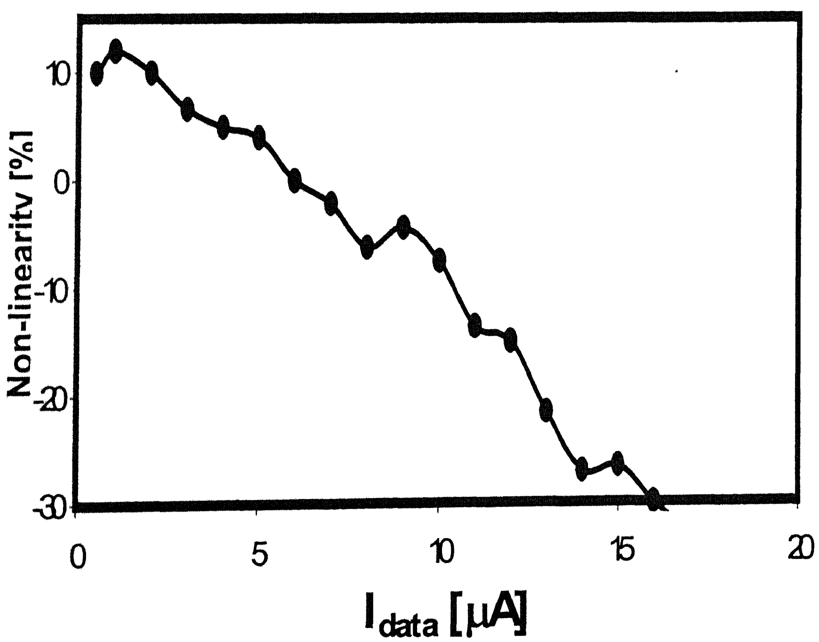


Figure 3.10: I_{data} vs Non-linearity

It can be seen that the output current variation **[Fig. 3.9]** due to the threshold voltage variation of the driving TFT is very minimal (< 2%) over a large change in threshold voltage (±40%). Thus the circuit performs well and effectively compensate for the threshold voltage variation of the order of ±40% or 2.5 ± 1volt as may be required by VGA display.

Also it can be noticed that the non-linearity in the output current **[Figure 3.10]** is fairly high and below 10% for data current range of about 8μA only. Thus the four TFT based pixel circuit eliminates the effect of threshold voltage variation in the driver TFT but has limited current range over which the output current matches well with the input current. This may limit the possible number of gray levels and hence the resolution. The reasons for these limitations are discussed in the subsequent sections.

3.4. Effects and Elimination of Clock-feedthrough in the pixel circuit

Clock-feedthrough is one of the dominant sources of error in switched-capacitor and switched-current circuits. It basically refers to coupling of clock (or control signals) through the parasitic gate-to-source and gate-to-drain capacitances of switching transistors to the output. In the circuit shown in **Figure 3.5**, the presence of parasitic capacitor C_{p1} between the gate and drain of TFT1 is the dominant source of error in the charge stored on storage capacitor C_S and therefore the output current. During charging of C_S, C_{p1} also gets charged up to voltage corresponding to node G voltage. At the end of programming period when TFT1 is switched off, the parasitic capacitor C_{p1} is unable to find any other discharge path except through the storage capacitor C_S thereby affecting its voltage. This voltage change has direct impact on the output drain current of TFT3.

It is observed that when the circuit is programmed with a data current through two ideal switches instead of the TFT1 and TFT2, the non-linearities in output current reduce drastically to less than 2% as shown in **Figure 3.11**. Thus it can be inferred that the main cause of output current non-linearity is the non-ideal nature of TFT1 and TFT2 primarily due to their associated parasitic capacitances.

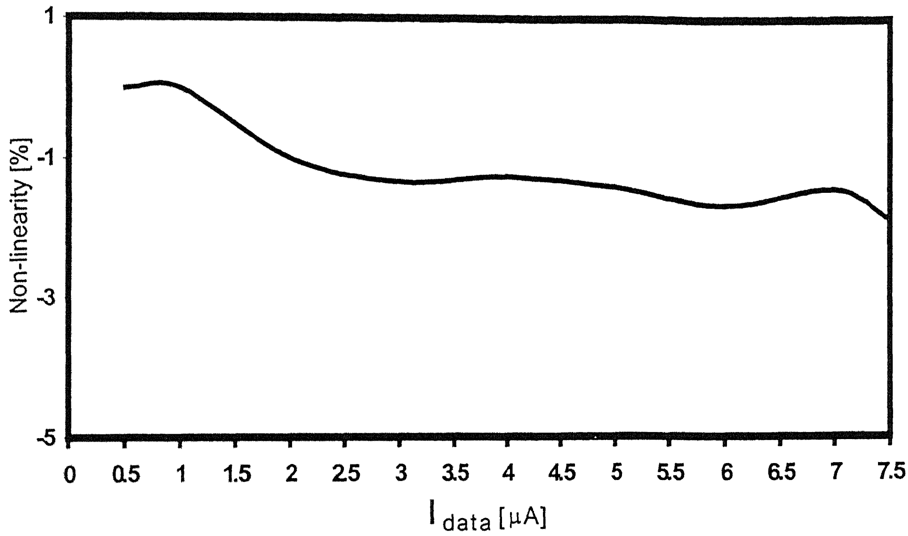


Figure 3.11: I_{data} vs Non-linearity using Ideal Switches

The effects of the parasitic capacitances can be determined by analyzing the circuit in **Figure 3.12,** which shows all the capacitances at the gate of the drive TFT3 [**Figure 3.5**]. Here, C_{gd3}, C_{gb3} and C_{gs3} are the parasitic capacitors associated with the TFT3 whereas C_{pl} is the gate-to-drain parasitic capacitor of the switching TFT1. V_d, V_s and $V_{a\text{-}Si}$ are the voltages at the drain, source and substrate of TFT3 respectively. The parasitic capacitor C_{pl} of TFT1 is primarily due to the overlap between TFT1's source/drain and gate electrodes. It causes TFT3's gate potential to drop when V_{select} is switched from VDD to 0V.

When V_{select} is 25V, node G is charged up to the data line voltage (V_{data}) by I_{data}. This voltage value is determined by the present current source voltage. Thus the charge stored at node G is

$$Q = C_{pl}\,(V_{data} - V_{select(ON)}) + C_{gd3}\,(V_{data} - V_d) + C_{gb3}\,(V_{data} - V_{a\text{-}Si}) + C_{gs3}\,(V_{data} - V_s) + C_S\,(V_{data} - V_{dd}) \qquad (3.1)$$

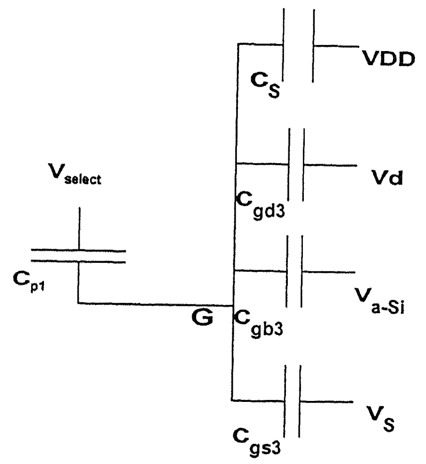


Figure 3.12: Capacitance equivalent circuit

If the source/gate and the drain/gate overlaps are identical in TFT3, we can assume $C_{gd3} = C_{gs3} = C_{p3}$, where C_{p3} represents TFT3 parasitic capacitance. C_{gb3} is the capacitance associated with gate over the field region and is equal to the gate-oxide capacitance (C_{OX}).

Eq (3.1) can be simplified as

$$Q = C_{p1}\,(V_{data} - V_{select(ON)}) + C_{p3}\,(2V_{data} - V_d - V_s) + C_{OX}\,(V_{data} - V_{a\text{-}Si}) + C_S\,(V_{data} - V_{dd}) \quad \ldots\ldots\ldots\ldots\ldots\ldots(3.2)$$

When V_{select} is switched to '0'V the charge stored at node G is

$$Q' = C_{p1}\,V' + C_{p3}\,(2V' - V'_d - V'_s) + C'_{gb}\,(V' - V'_{a\text{-}Si}) + C_S\,(V' - V_{dd}) \quad \ldots..(3.3)$$

Where V' represent the potential at node G after V_{select} is switched from 25V to 0V. Now C'_{gb3} would remain same as C_{OX}, if TFT3 remains in saturation. Assuming that TFT3 field region ($V_{a\text{-}Si}$) and drain and source potential changes are negligible after each switching, Eq (3.3) can be re-written as

$$Q' = C_{p1}\,V' + C_{p3}\,(2V' - V_d - V_s) + C'_{OX}\,(V' - V'_{a\text{-}Si}) + C_S\,(V' - V_{dd}) \quad \ldots\ldots(3.4)$$

Now, Q' will be equal to Q if there are no charge leakage from node G back to the data line through TFT1 in the reproduction stage. Thus substituting Eq (3.4) into Eq (3.2) and replacing ($V_{data} - V'$) by ΔV, which is the change in voltage at node G, we get

$$\Delta V = (C_{p1}\ \Delta V_{select}) / (C_{p1} + 2\ C_{p3} + C_{OX} + C_s) \quad \textbf{(3.5)}$$

Where, ΔV_{select} is the voltage change in V_{select} terminal.

The analysis shows that the change ΔV in the voltage of node G depends on the parasitic capacitance C_{p1} and storage capacitance C_S. If it is assumed that TFT1 switches off instantaneously when V_{select} is made low, then using eq. (**3.5**) we see that clock-feedthrough can be minimized by increasing the storage capacitor C_S. However, this would also increase the time required to charge the capacitor thereby limiting the number of matrix rows and hence the resolution of the display panels. Reduction in width of TFT1 can also reduce the capacitance but it would also increase its resistance, thereby adversely affecting the linearity of the transfer characteristics as shown later.

While obtaining Eq. (**3.5**), it was assumed that when the signal at the gate of TFT1 is made low, it switches off and becomes non-conducting immediately, thereby leaving no other path for C_{p1} to discharge except through C_S. Let us now consider the situation at node G immediately after the termination of programming period. The effect of TFT2's parasitic capacitance comes into picture now as they are

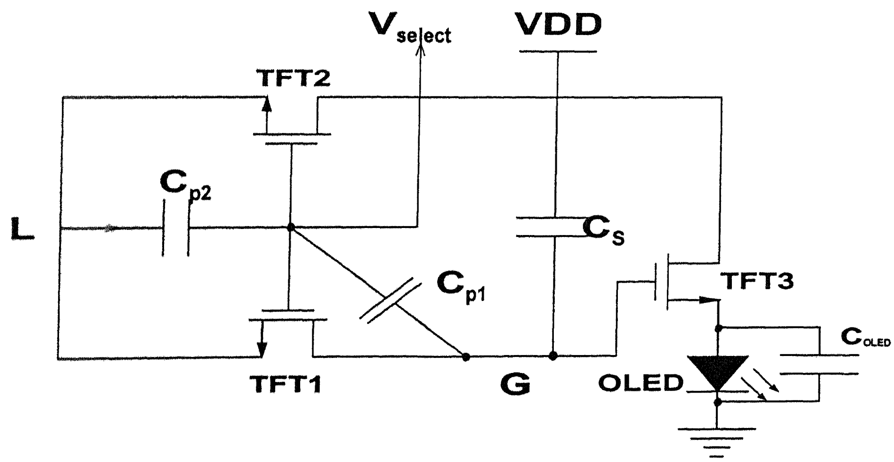


Figure 3.13: Switching Equivalent Circuit

also charged up and need to be discharged after programming. **Figure 3.13** shows these capacitances as lumped single capacitance C_{p2}. After programming is complete and V_{select} has gone low and the programming current pulse has died down, the potential at node L will go to a negative potential value. This will make TFT1 and TFT2 to turn ON by biasing their gate-to-source voltage to greater than the threshold voltage as required to turn ON a transistor. As a consequence, the transistors TFT1 and TFT2 remain conducting for a very short period so as to provide discharge paths for these parasitic capacitances. If this time period can be enhanced then a considerable part of charge on C_{p1} also can flow through TFT1 rather than through the storage capacitor. Since the transistors remain open basically to provide discharge paths for parasitic capacitance C_{p2}, an increase in the value of these capacitances will achieve the desired result. This can be done by increasing the size of TFT2. Extensive simulations confirmed this and it is seen that the aspect ratio (W/L) of TFT2 should be approximately 10 times larger than that of TFT1 so that C_{p2} substantially increased to minimize the non-linearity in output current. This will improve the achievable output current range of the pixel circuit.

3.5. Simulations of Improved circuit using Amorphous Silicon TFT

The circuit of **Figure 3.5** is simulated with the improved transistor sizes as shown in **Table 3.2**. In the first row, the TFT sizes as reported in **[6-8]** are shown. In the second row of **Table 3.2**, the TFT sizes for improved design keeping in mind the clock-feedthrough effects as illustrated in last section are shown. The W/L of TFT2 is selected as 500μm/6μm instead of 100μm/6μm to increase C_{p2}. The third row shows a set of TFT sizes to demonstrate that scaling the width of TFT1 does not solve the problem. Here W/L of TFT2 is kept as it is and W/L of TFT1 is reduced to 10μm/6μm. The fourth row contains TFT sizes to justify the parameters of second row properly as explained later.

Figure 3.14 shows the plot of non-linearity in output current vs. the input current I_{data} under all the above mentioned four cases. The curve '**a**' shows performance of the circuit as shown in **Fig 3.10** also. The current range over which non-linearity is less than 10% is about 8 μA.

TABLE 3.2: Improved Design Parameters for Amorphous Silicon TFT

VDD = 25 Volts; V_{select} = 0 – 25V ; V_{ctl} = 0-25V; I_{data} = 0-20 μA

Parameters	TFT1 (W/L)	TFT2 (W/L)	TFT3 (W/L)	TFT4 (W/L)	C_{OLED}	C_S
Parameters for Basic Circuit (Curve 'a')	50μm/6μm	100μm/6μm	250μm/6μm	250μm/6μm	6 pF	6 pF
Parameters for Improved Circuit (Curve 'c')	50μm/6μm	**500μm/6μm**	250μm/6μm	250μm/6μm	6 pF	6 pF
Parameters for Changed Circuit (Curve 'b')	**10μm/6μm**	100μm/6μm	250μm/6μm	250μm/6μm	6 pF	6 pF
Parameters for Changed Circuit (Curve 'd')	**16μm/2μm**	500μm/6μm	250μm/6μm	250μm/6μm	6 pF	6 pF

Next the circuit was simulated using the parameters mentioned in Row 2 of **Table 3.2**. These TFT sizes were arrived at based on the results of the analysis discussed in the previous section and extensive simulations with various TFT sizes. Curve **'c'** shows the performance of the circuit where we can clearly see the improvement in the non-linearity (<< 10%) of output current for a range as high as 20 μA.

Curve **'b'** was obtained using the data shown in Row 3 of **Table 3.2**. In this case the W/L of TFT1 was reduced to 10μm/6μm, keeping the W/L of TFT2 same. The curve **'b'** shows that decreasing C_{p1} through TFT1 cannot enhance the output current range. Since the ON-resistance of TFT1 is dependent on the W/L ratio inversely, it affects the circuit's performance. This point is also demonstrated by adjusting the W/L ratio of TFT1 to 16μm/2μm as shown in Row 4 of Table 3.2, thus reducing the ON resistance of TFT1. Curve **'d'** shows the performance of the circuit under the above condition, which is almost same as that of curve **'c'**.

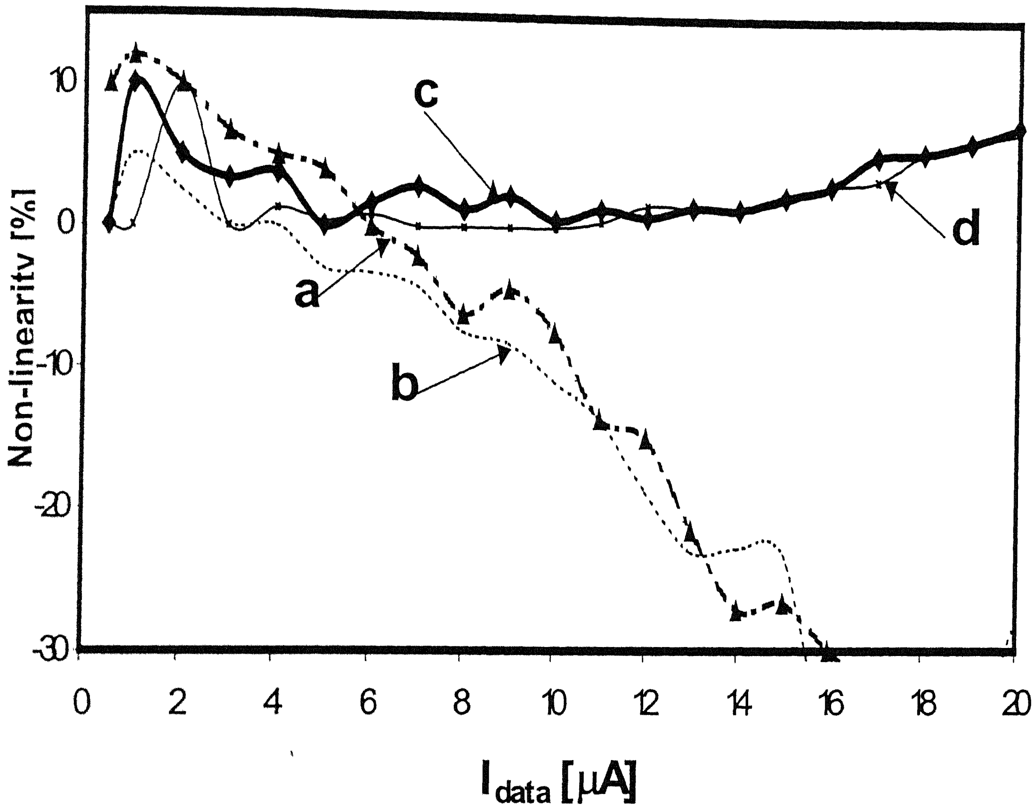


Figure 3.14: I_{data} vs Non-linearity for circuit of Fig. 3.5

Besides the drive TFT, the variations in the threshold voltage of switching TFTs have no major impact in the output characteristics of the pixel circuit. However the variations in the threshold voltage of the load TFT affects the output current range as discussed below.

In **Figure 3.15** the output current under various threshold voltage variations are plotted. The device sizes used are as shown in Row 2 of Table 3.2. The worst case output

current range from the circuit is expected when the threshold voltages of transistors increase. In **Figure 3.15,** Curve **1** shows the output current if drive TFT's threshold voltage is increased to 3.5 V, keeping threshold voltages of rest of TFTs unchanged i.e at 2.5V. This shows that output current starts deviating from the ideal value at about I_{data} =16 μA.

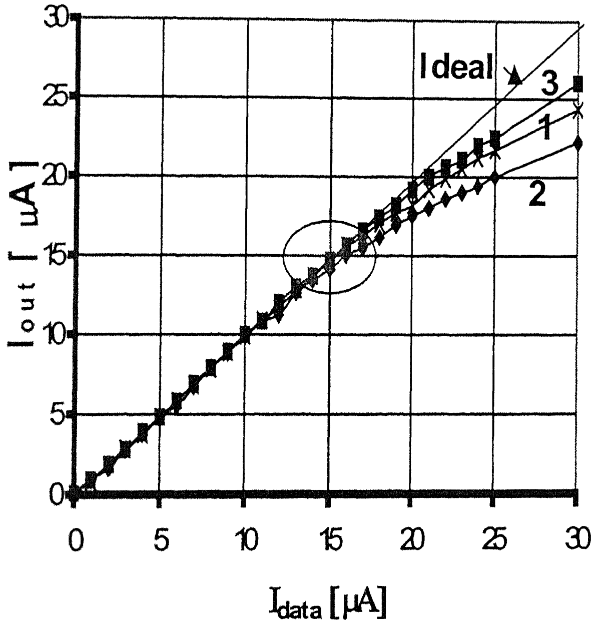


Figure 3.15: I_{data} vs I_{out} for circuit of Fig.3.5

Curve **2** shows the output current when the load TFT's threshold voltage is 3.5 volts keeping all other TFT's threshold voltage at 2.5V. The curve **3** shows the effect of increasing the threshold voltage of the switching TFTs to 3.5V, keeping the load and drive TFTs threshold voltage to 2.5V.

These plots and analysis shows that the increase in load TFT's threshold voltage reduces the output current range that can be achieved. This means that as the voltage drop across the load TFT increases, less output current range is expected from the circuit. This is presented in detail in the next section.

3.6. Enhancement in Output Current by Operating the Load TFT in Triode Regime

Apart from clock-feedthrough, another factor, which limits the current range, is the transition of TFT3 [**Figure 3.5**] from saturation to triode region mode of operation as a result of increased voltage drop across TFT4 as the input data current increases. Let us assume for the sake of simplicity, TFTs can be modeled as bulk MOSFETs. Since TFT3 (n-type) always works in the saturation regime in the useful range of the circuit of **Figure 3.5**, the drop across its drain and source is at least $\Delta V_{TFT3.}$ Since the gate of TFT4 is at VDD when the device in ON, its source voltage required to maintain a current is $(V_{thN} + \Delta V_{TFT4})$. Now the voltage drop across TFT4-TFT3-OLED combination can be written as

$$VDD \geq (V_{thN} + \Delta V_{TFT4}) + \Delta V_{TFT3} + V_{OLED} \qquad \textbf{(3.6)}$$

Where,

VDD is the Power Supply voltage,

V_{thN} is the threshold voltage of N-channel TFT,

ΔV_{TFT3} is the drain-to-source voltages for TFT3,

ΔV_{TFT4} is the drain-to-source voltages for TFT4 and

V_{OLED} is the voltage drop across the OLED.

Eq (3.6) can be re-written as

$$\Delta V_{TFT3} \leq [VDD - V_{OLED} - (V_{thN} + \Delta V_{TFT4})] \qquad \textbf{(3.7)}$$

Since a certain minimum value of ΔV_{TFT3} is necessary for maintaining TFT3 in saturation, an increase in ΔV_{TFT3} will extend the range of current over which the circuit will work satisfactorily. Analysis of Eq. (3.7) shows that this can be achieved by reducing the voltage drop $(V_{thN} + \Delta V_{TFT4})$. In the circuit shown in **Figure 3.5**, $(V_{thN} + \Delta V_{TFT4})$ is fairly large because the transistor (TFT4) is forced to work in saturation. However, if this transistor is replaced by a P-type transistor as shown in **Figure 3.16**, then the transistor can be forced to work in triode region where voltage drop across it will be smaller. Another benefit of replacing TFT4 with a P-type transistor is that the control signal V_{select} can be directly used to turn it ON and OFF thereby reducing either one control line or additional two transistors (with 'inverter' configuration) that would otherwise have been required **[6]**.

Since a P-type transistor is not available in amorphous Silicon technology, the proposed circuit is best implemented using Polysilicon transistors. As a result of reduced voltage drop across transistor P1 and reduction of clock-feedthrough effects using the technique outlined earlier, it is expected that the new circuit will have a much better transfer characteristics. Further, the transistor sizes and supply voltages can also be reduced because of better mobility of Polysilicon devices.

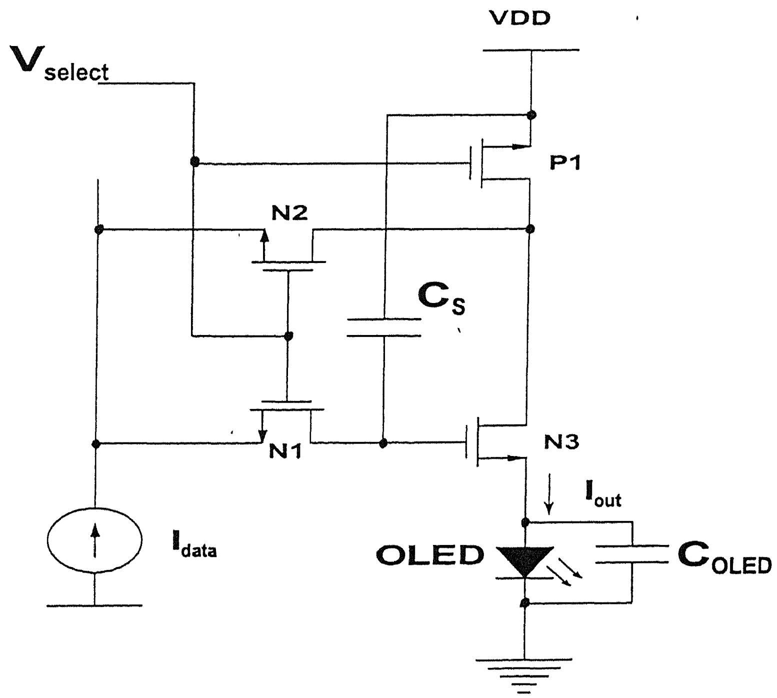


Figure 3.16: Improved pixel circuit using Polysilicon TFTs

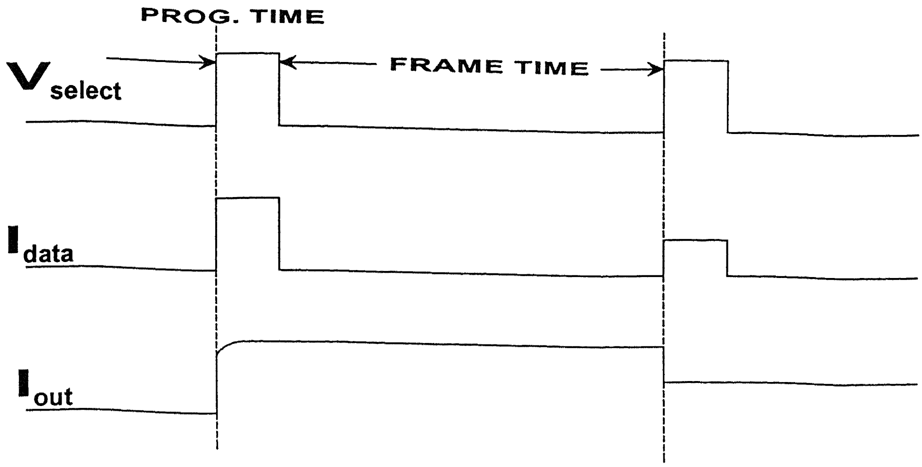


Figure. 3.17: Operation Waveform for Polysilicon TFT based Pixel Circuit

The improved circuit configuration of **Figure 3.16** was simulated and studied using polysilicon TFT model parameters from AIM-SPICE. The design parameters are given in **Table 3.3**. The details of the model parameters (PSIA-2 Level-16) are included in **Appendix-A**. Due to the higher mobility of Polysilicon devices, higher output current range can be achieved even using lower supply voltage (10V).

TABLE 3.3: Design Parameters for Polysilicon TFT

VDD = 10 Volts; V_{select} = 0 – 15V ; I_{data}= 0-30 μA

Parameters for Improved Simulation	$(W/L)_{N1}$	$(W/L)_{N2}$	$(W/L)_{N3}$	$(W/L)_{P1}$	C_{OLED}	C_S
	20μm/2μm	80μm/2μm	250μm/6μm	230μm/6μm	6.4 pF	6.61 pF

3.7. Simulation of improved circuit using Polysilicon TFT

The polysilicon TFT based circuit was simulated using level 16 polysilicon TFT parameter in AIM-SPICE circuit simulator. The output current was measured at the cathode terminal of the OLED. The non-linearity in output current is plotted against the input data current I_{data} in **Figure 3.18**. It is clear from the curve that the improved output current range of about 25 μA with less than 5% non-linearity is achieved through this circuit. The improvement has come due to the improved design features such as transistor sizing considering the clock feedthrough effects. Also the ΔV of the drive TFT got increased due to the use of P-type load TFT as illustrated in the enhancement factors in the previous section.

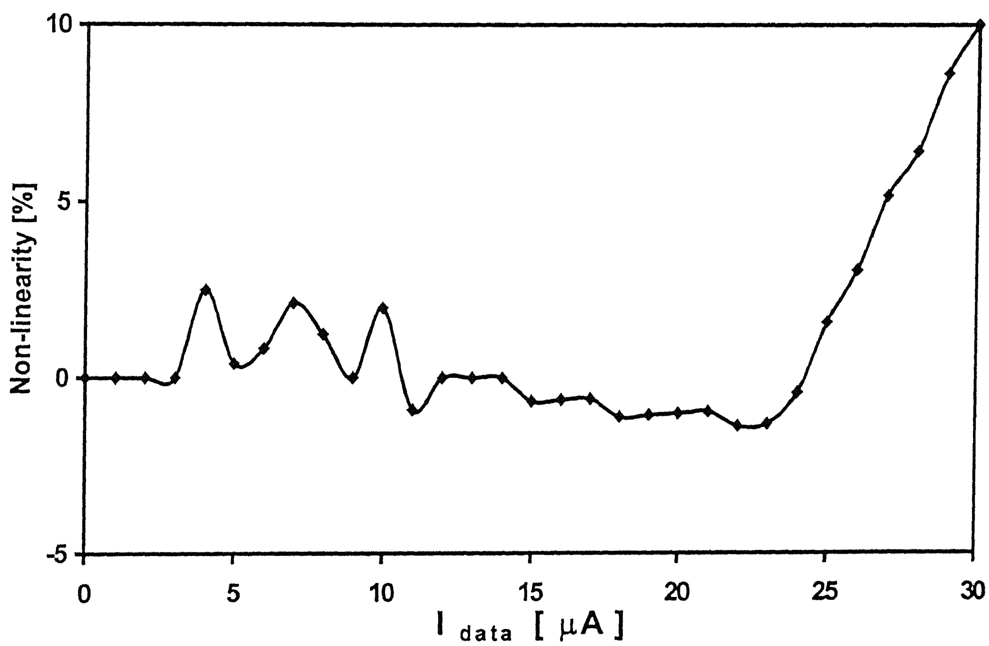


Figure 3.18: I_{data} vs Non-linearity for P-Si TFT circuit [Figure 3.16]

3.8. Limitations of the current pixel circuits

The major limitations of the current pixel circuit are the following:

1. One of the basic conditions for the pixel circuit to work properly is that the drive TFT should always work in saturation. This TFT can be thought of an ideal current source with very high output resistance in parallel while working in saturation. On the other hand, when the TFT works in linear regime it's output resistance drops drastically and thus cease to operate as a current source. Referring to **Figure 3.19,** which shows the I_{ds}-V_{ds} characteristics of the drive TFT, we see that with the application of a high magnitude data current pulse during programming, the voltage at the gate (V_G) of the driver transistor N3 increases to a large value approaching

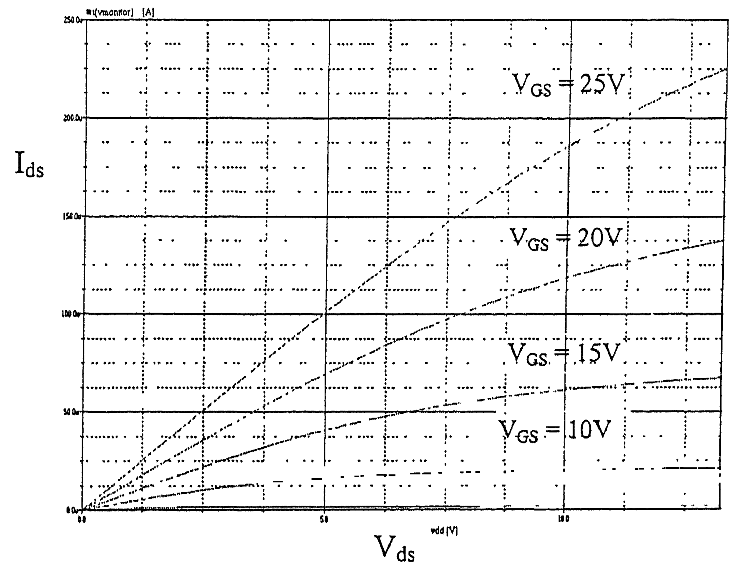


Figure 3.19: I_{ds} –V_{ds} characteristics of the drive TFT (N3) of Figure 3.16

VDD. But during reproduction phase the drain voltage of N3 will drop much lower value than V_G due to high current flowing through P1 thus forcing the transistor N3 to work in linear regime.

In the **Figure 3.19** the I_{ds} curve corresponding to V_{GS}=20V is showing that the drive TFT's output resistance drops drastically. Under this condition the output current non-linearity increases to intolerable level because the TFT does not work as current source. But the case of I_{ds} curve corresponding to V_{GS}=10V or V_{GS}=15V the TFT has very high output resistance and works as current source

2. The other limitation comes at very low value data current pulses. Here the problem is in the development of the required voltage at the gate of N3 (that is to charge up C_S) to turn it ON. The programming time may not be sufficient in this case and hence the pixel circuit ceases to operate properly.

3.9. Design of Voltage Pixel Circuit

The functioning of simple voltage pixel circuit of **Figure 2.3** has been explained earlier. This circuit with polysilicon TFTs was simulated using AIM-SPICE circuit simulator to evaluate the performance. The simulation results are plotted in **Figure 3.20.**

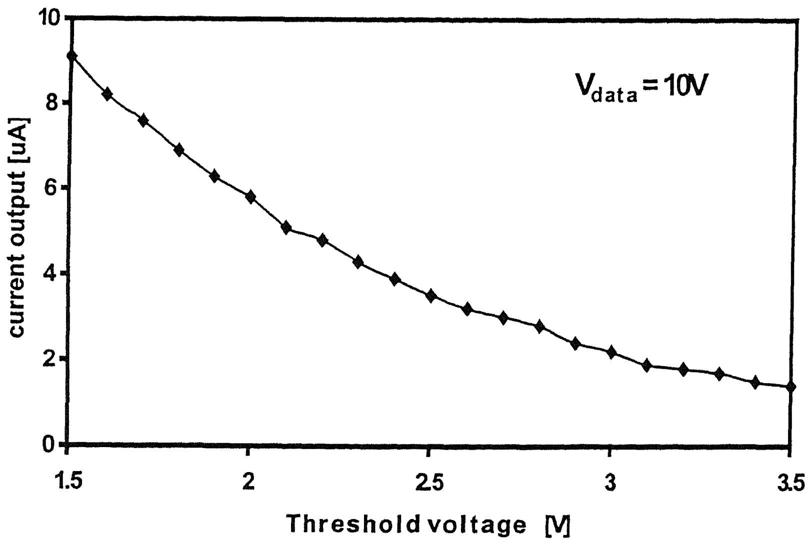


Figure 3.20. Variation of output current for Simple Voltage Pixel Circuit

It can be seen that for a constant data voltage of 10 volts the output current varies by as much as 100% for threshold voltage variation of ±1Volt. This shows that the circuit is very sensitive to the threshold voltage variation of the driver transistor T2.

3.10. Basic Principle of Operation of Improved Voltage Pixel Circuit

The improved **[18]** voltage pixel circuit **[Figure 3.21]** uses five transistors and two capacitors. It has six external lines including VDD and Ground, which can be shared among pixels. Also $V_{AZ(Prev)}$ is in strict sense not an external line but comes from an adjacent pixel. The relationship among the waveforms are shown in **Figure 3.22.**

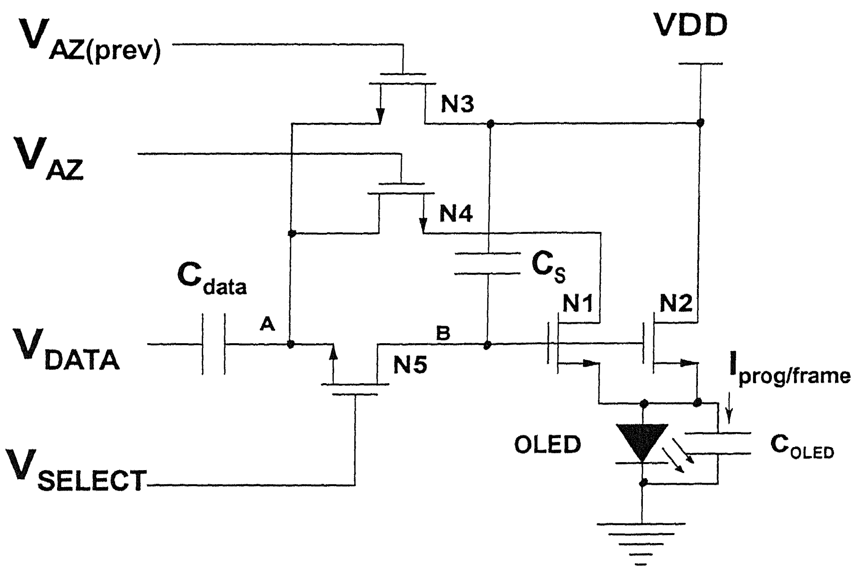


Figure 3.21: Voltage pixel circuit Schematic

The circuit has three phases of operation namely (1) Precharge phase, (2) Autozero phase and (3) Data writing phase.

1) **Precharge phase**: The first phase is the precharge phase, where $V_{AZ(Prev)}$ is made high which turns on transistor N3 and precharges node A upto a voltage slightly less than VDD. Then the data line changes from its baseline value to write data into the pixel of the previous Row. This has no effect on the pixel under consideration.

2) **Autozero phase:** The second phase is the Auto-zero phase. The V_{AZ} and V_{SELECT} lines for the present row go high, turning 'ON' transistors N4 and N5, causing the gate of N1 to drop, self biasing to a turn-on voltage that permits a very small amount of current to flow through OLED.

The sum of turn-on voltage of OLED and the threshold voltage of N1 are stored on the gate of N1. Threshold voltages of N1 and N2 will be similar since they can be placed very close to each other. Also the gate-to-source voltage (V_{GS}) will be same. Since TFT threshold drift depends only on V_{GS}, it is assumed that the threshold voltage of these devices will track each other. Thus the threshold voltage of N2 is also stored on its gate. After completion of auto-zero, the V_{AZ} line returns to low, while V_{SELECT} stays high.

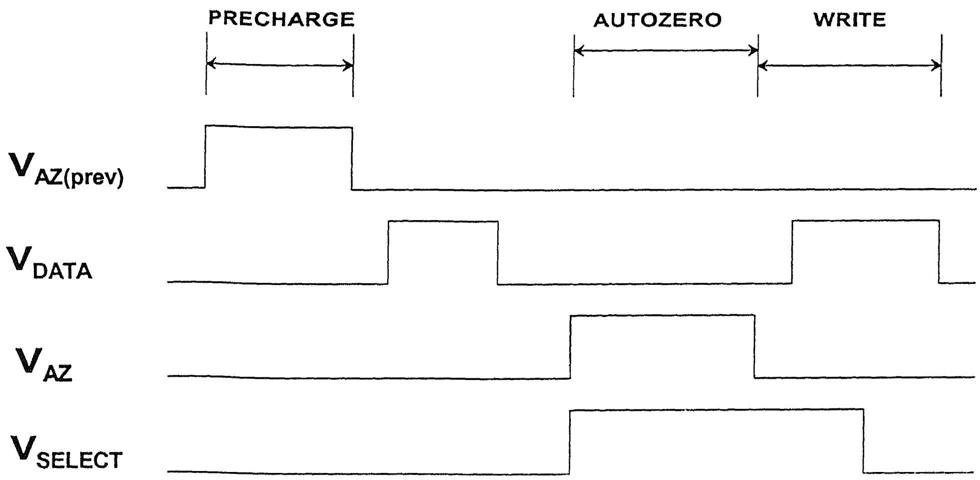


Figure 3.22: Voltage Pixel Circuit Input Waveforms

3) **Data writing phase**: The final phase is data writing. The data is applied as a voltage V_{DATA} above the baseline of the data line and written through the capacitor C_{data}. Afterwards the select line returns low, and the sum of data voltage, plus N2's threshold voltage is stored at node B for the rest of the frame. A storage capacitor (C_S) is put in node B to protect the voltage at node B from leaking away.

3.11. Design Analysis of the Voltage Pixel Circuit

The voltage pixel circuit **[Figure 3.21]** can be designed by keeping in mind the role of each transistor and capacitor. The precharge transistor (N3) is used to charge up the node A close to VDD. The aspect ratio (W/L) should be such that the drain-to-source drop across N3 should be small and it should work in the triode regime. The transistor N4 is

used to auto-zero the circuit as described earlier. This device will bias N1 in saturation region and hence the W/L ratio of this transistor (N4) should be considerably high.

The transistor N5 is used as the access transistor. It joins the 'critical node' B with A while during autozero as well as while loading the data. The parasitic capacitors of this transistor cause clock-feedthrough and thus to be minimized. But the aspect ratio should not be very less also because in that case the drop across the transistor will be high and this will limit the effective data voltage range.

N2 is used as driver to the OLED, while N1 helps during auto zeroing. During auto-zero phase, the transistor N1 is forced to work in saturation and after that it comes back to linear region. Since the threshold voltages of N1 and N2 track each other, their aspect ratios (W/L) should be desirably same. The (W/L) of N1 and N2 can be decided based on the drive output and channel length modulation factor.

. The crucial role of C_S is that it stores the voltage of the critical node B. If the value of C_S is large it helps in eliminating clock feedthrough effects. At the same time it will store large voltage after auto-zero cycle thus limiting the useful input voltage range because it can utmost be charged upto VDD during data loading phase. The best value of C_S is very close to the OLED parasitic capacitor. Thus it can store un-ambiguous voltage in the presence of the parasitic capacitors of N1 and N2.

The role of the data capacitor is to couple the input data voltage. It also holds the precharge voltage. The autozero cycle should be quick enough to make the pixel operation fast. During autozero cycle the stored charge in C_{data} moves to the gate of N1 to self-bias the OLED to a small current. Thus C_{data} should be moderate value capacitor (~1pF). If C_{data} is made large then, we will loose useful data voltage range, since C_S can be charged upto only VDD.

It should be noted that the data voltage increment applied to the data line does not appear directly across the OLED, but split between V_{GS} of N2 and the OLED. This means there is non-linear mapping from data voltage to the OLED voltage. This mapping combined with the non-linear mapping from OLED voltage to OLED current will yield the overall transfer function from data voltage to OLED current, which is monotonic.

3.12. Simulation of Voltage Pixel Circuit

The voltage pixel circuit was simulated and studied using the Polysilicon TFT parameters in Microcap Spice Simulator. The design parameters are shown in **Table 3.4**. These parameters were arrived at based on the analysis of the circuit and repeated simulations.

TABLE 3.4: Design Parameters for Voltage Pixel Circuit

VDD = 10 Volts; $V_{AZ(PREV)}$ = 0 – 10V; V_{AZ} = 0 – 10V; V_{SELECT} = 0 – 10V;

$(W/L)_{N1}$	$(W/L)_{N2}$	$(W/L)_{N3}$	$(W/L)_{N4}$	$(W/L)_{N5}$	C_{data}	C_S	C_{OLED}
20μm/1μm	20μm/1μm	20μm/1μm	20μm/1μm	10μm/1μm	1pF	6pF	6pF

The voltage pixel circuit was simulated using the signals as shown in **Figure 3.22**. With the application of data voltage pulse of different voltages (0 to 20 Volts) the output current at OLED cathode was measured during the 'writing time' as well as during the frame time. The current non-linearity in this case was calculated as the difference between the currents during the writing time (I_{prog}) and the frame time (I_{frame}) expressed in percentage. So the output current non-linearity of the circuit can be expressed as

$$\text{Non-linearity} = [(I_{prog} - I_{frame}) / I_{prog}]\ \%$$

Figure 3.23 shows the plot of input voltage versus non-linearity as obtained from the circuit. It can be seen that at higher data voltage the output current non-linearity is high. At the lower data voltage range (0-10 volts) the non-linearity is less than 2%. Also it can be seen that [**Figure 3.24**] the current output is fairly linear even with the threshold voltage variation of +/- 1 Volt from the nominal value of 2Volts.

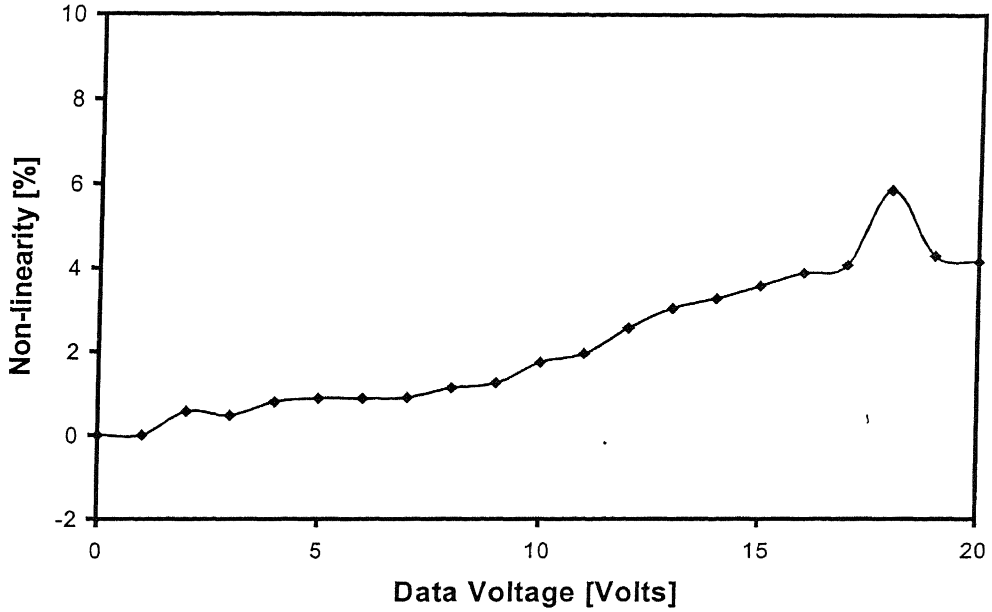


Figure 3.23: V_{data} vs. Non-linearity for Voltage Pixel Circuit [Figure 3.21]

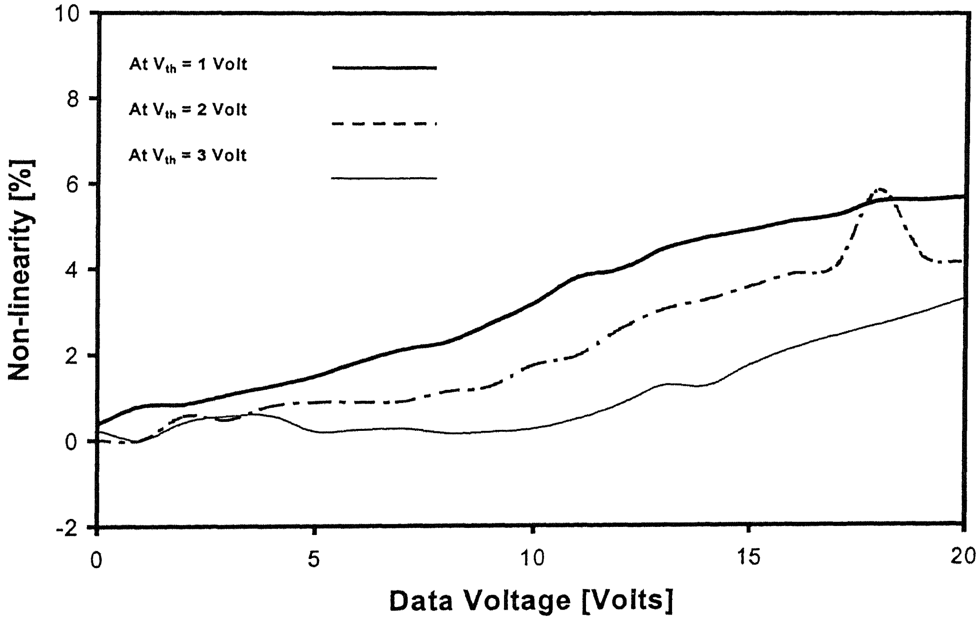


Figure 3.24: V_{data} vs. Non-linearity for Voltage Circuit at different V_{th}

Chapter - 4

CONCLUSIONS

4.1. Impact of the Research in Display Technology

The major interests in OLED displays are due to the possibility of large area, high-resolution displays to provide low cost alternative to LCD displays. To achieve this goal, Active Matrix OLED display is seemingly the best solution. The design of pixel circuit associated with OLED is crucial to the overall performance of the display.

In this work we have shown that the circuits proposed so far are able to reduce the effect of spatial variation of threshold voltage of TFTs but they have a limited current range over which the output current matches well with the data current. Based on detailed analysis and simulations we have shown that the source of this problem is primarily the clock feedthrough effect. Based on our analysis we have proposed a new technique for sizing the TFTs that reduces this effect successfully. We have shown that the useful current range can be increased by almost a factor of three.

We also show in this work that by using a P-type load, the current range of the circuit can further be increased. Based on this result we have proposed a new four polysilicon TFT based circuit that has a current range 25 μA at supply voltage of 10 Volts only. It has the added advantage of using only four external lines.

4.2. Extension to the Research

During this thesis work, the Current driven pixel circuits were studied in great detail and improvements in reported pixel circuits were suggested. Although the reported voltage driven circuits work reasonably well, they have complicated mode of operation. A simplification of this could aid in more wide spread use of these voltage driven circuits.

The results of the present work can also be utilized in the design of the Dynamic current mirrors or Current copiers for the Switched-Capacitor technology. The concept of reduction of clock feedthrough by sizing the transistors will be attractive to many due to the simplicity it offers in circuit design.

Appendix – A

Table A-1: Model Parameters for a-Si TFT (Level 15)

Sl. No.	Name	Parameter	Value (unit)
1.	ALPHASAT	Saturation modulation parameter	0.6
2.	CGDO	Gate-drain overlap capacitance per meter channel width	0 F/m
3.	CGSO	Gate-source overlap capacitance per meter channel width	0 F/m
4.	ASAT	Proportionality constant of Vsat	1
5.	DEF0	Dark Fermi level position	0.6 eV
6.	DELTA	Transition width parameter	5
7.	EL	Activation energy of the hole leakage current	0.35 eV
8.	EMU	Field effect mobility activation energy	0.06 eV
9.	EPS	Relative dielectric constant of substrate	11
10.	EPSI	Relative dielectric constant of gate insulator	7.4
11.	GAMMA	Power law mobility parameter	0.4
12.	GMIN	Minimum density of deep states	$1E^{23}$
13.	IOL	Zero bias leakage current	$3E^{-14}$ A
14.	KASAT	Temperature coefficient of ALPHASAT	0.006 1/°C
15.	KVT	Threshold voltage temperature coefficient	-0.036 V/°C
16.	LAMBDA	Output conductance parameter	0.0008 1/V
17.	M	Knee shape parameter	2.5
18.	MUBAND	Conduction band mobility	0.001 m^2/V-sec
19.	RD	Drain resistance	0.0 W
20.	RS	Source resistance	0.0 W
21.	SIGMA0	Minimum leakage current parameter	1E-14 A
22.	TNOM	Parameter measurement temperature	27°C
23.	TOX	Thin-oxide thickness	3.0e-7 m
24.	V0	Characteristic voltage for deep states	0.12 V
25.	VAA	Characteristic voltage for field effect mobility (determined by tail states)	7.5E3 V
26.	VDSL	Hole leakage current drain voltage parameter	7 V
27.	VFB	Flat band voltage	-3 V
28	VGSL	Hole leakage current gate voltage parameter	7V
29.	VMIN	Convergence parameter	0.3 V
30.	VTO	Zero-bias threshold voltage	2.5V

Table -A2: Model Parameters for Polysilicon TFT (Level 16)

Sl. No.	Name	Parameter	Value (unit)
1.	ASAT	Proportionality constant of Vsat	1
2.	AT	DIBL parameter 1	3E-8 m/V
3.	BLK	Leakage barrier lowering constant	0.001
4.	BT	DIBL parameter 2	1.9E-6 m·V
5.	CGDO	Gate-drain overlap capacitance per meter channel width	0 F/m
6.	DASAT	Temperature coefficient of ASAT	0 1/°C
7.	DD	Vds field constant	1400 Å
8.	DELTA	Transition width parameter	4.0
9.	DG	Vgs field constant	2000 Å
10.	DMU1	Temperature coefficient of MU1	0
11.	DVT	The difference between VON and the threshold voltage	0 V
12.	DVTO	Temperature coefficient of VTO	0 V/°C
13.	EB	Barrier height of diode	0.68 EV
14.	ETA	Subthreshold ideality factor	7
15.	ETAC0	Capacitance subthreshold ideality factor at zero drain bias	ETA
16.	ETAC00	Capacitance subthreshold coefficient of drain bias	0 1/V
17.	I0	Leakage scaling constant	6.0 A/m
18.	I00	Reverse diode saturation current	150A/m
19.	LASAT	Coefficient for length dependence of ASAT	0 M
20.	LKINK	Kink effect constant	19E-6 M
21.	MC	Capacitance knee shape parameter	3.0
22.	MK	Kink effect exponent	1.3
23.	MMU	Low field mobility exponent	3.0
24.	MU0	High field mobility	100(NMOS), 50(PMOS) cm^2/ V-sec
25.	MU1	Low field mobility parameter	0.0022
26.	MUS	Subthreshold mobility	1.0
27.	RD	Drain resistance	0.0 W
28.	RDX	Resistance in series with Cgd	0 W
29.	RS	Source resistance	0.0 W
30.	RSX	Resistance in series with Cgs	0.0 W
31.	TNOM	Parameter measurement temperature	27°C
32.	TOX	Thin-oxide thickness	1.0e-7 m
33.	VFB	Flat band voltage	0.1 V
34.	VKINK	Kink effect voltage	9.1 V
35.	VON	On-voltage	0 V
36.	VTO	Zero-bias threshold voltage	2.5 V

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